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Patent

Docket No.: CYPR-CD00190

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.			
Date of Deposit:	02/24/03	Name of Person Making the Deposit:	KATHERINE RINALDI
		Signature of the Person Making the Deposit:	<i>Katherine Rinaldi</i>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

3-10-03

Inventor(s): Bert Sullam

Serial No.: 09/826,397

Group Art Unit:

Filed: 04/02/01

Examiner:

Title: METHOD AND CIRCUIT FOR ALLOWING A MICROPROCESSOR TO CHANGE ITS OPERATING FREQUENCY ON-THE-FLY

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

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MAR 04 2003

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

Technology Center 2100

- Formal drawings, totaling sheets.
- Informal drawings, totaling sheets.
- Certification for PTO Consideration
- Information Disclosure statement (___ sheets)
- ☒ Information Disclosure statement and late filing fee
- ☒ Form 1449
- Petition for Extension of Time
- ☒ Other: REFERENCES
- ☒ Other: Related US Pending Patent Applications

Fee Calculation (for other than a small entity)					
Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere)				\$.00	\$0.00
Information Disclosure Statement, late filing				\$180.00	\$180.00
Other:					\$0.00
Total Fees					\$180.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:
 - ☒ The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085.
A duplicate copy of this authorization is enclosed.
 - ☒ A check in the amount of \$180.00
 - ☐ Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:


WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

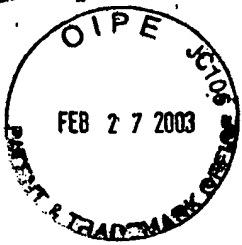
Date: _____

2/24/2003

By: _____



Anthony C. Murabito
Reg. No. 35,295



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00190

RECEIVED

Inventor(s): Bert Sullam

Serial No.: 09/826,397

Group Art Unit:

MAR 04 2003

Filed: 04/02/01

Examiner:

Technology Center 2100

Title: METHOD AND CIRCUIT FOR ALLOWING A MICROPROCESSOR TO CHANGE ITS
OPERATING FREQUENCY ON-THE-FLY

The Commissioner of Patents and Trademarks

Washington, D.C. 20231

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
6,144,327	PROGRAMMABLY INTERCONNECTED PROGRAMMABLE DEVICES	11/07/00
5,202,687	ANALOG TO DIGITAL CONVERTER	04/13/93
6,166,367	PROGRAMMABLE ANALOG ARITHMETIC CIRCUIT FOR IMAGING SENSOR	12/26/00
5,600,262	INTEGRATED CIRCUIT FACILITATING SIMULTANEOUS PROGRAMMING OF MULTIPLE ANTIFUSES	02/04/97
5,414,308	HIGH FREQUENCY CLOCK GENERATOR WITH MULTIPLEXER	05/09/95
5,258,760	DIGITALLY DUAL-PROGRAMMABLE INTEGRATOR CIRCUIT	11/02/93
5,563,526	PROGRAMMABLE MIXED-MODE INTEGRATED CIRCUIT ARCHITECTURE	10/08/96
6,225,866	SERIES CONNECTED MULTISTAGE LINEAR FET AMPLIFIER CIRCUIT	05/01/01

03/03/2003 CNGUYEN 00000043 09826397

01 FC:1806

180.00 OP

The Examiner's attention is respectfully directed to the following Related Pending U.S. Patents/Applications:

CYPR-CD00175; "METHOD FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE PROGRAMMABLE ANALOG BLOCKS (AS AMENDED)"; 10/01/01; 09/969,311; B. Sullam

CYPR-CD00189; "SYSTEM AND METHOD OF PROVIDING A PROGRAMMABLE CLOCK ARCHITECTURE FOR AN ADVANCED MICROCONTROLLER"; 10/24/01; 10/000,383; Sullam et al.

CYPR-CD00190; "METHOD AND CIRCUIT FOR ALLOWING A MICROPROCESSOR TO CHANGE ITS OPERATING FREQUENCY ON-THE-FLY"; 04/02/01; 09/826,397; B. Sullam

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Respectfully submitted,

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2/24/2003

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Anthony C. Murabito
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